

**In the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended): A graphics processing engine, comprising:

a rendering engine processing core for receiving graphics primitives an incoming data stream and converting them to pixel information it to output information in a predetermined format for transfer to a display an output device, said rendering engine processing core operable to access memory locations with multiple memory access requests for a Read or a Write operation and operable in a first address space;

a plurality of memory blocks, each individually accessible and all of said plurality of memory blocks configured in a virtual address space different than said first address space;

a memory mapping device for mapping each of said memory requests to the virtual address space; and

a pipeline engine for pipelining said mapped memory access requests for both Read and Write operations in accordance with a predetermined pipelining scheme, said memory access requests received in parallel and processed asynchronously, such that access to more than one of said memory blocks can occur at substantially the same time.

2.(Currently Amended): The graphics processing engine of Claim 1, wherein said rendering engine processing core, said memory mapping device, said pipeline engine and at least a portion of said plurality of memory blocks are contained within a common bounded space with limited connectivity to external peripheral devices.

3.(Currently Amended): The graphics processing engine of Claim 2, wherein said plurality of memory blocks includes at least one block of external memory external to said common bounded space.

**AMENDMENT AND RESPONSE**

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4.(Currently Amended): The graphics processing engine of Claim 2, wherein said common bounded space comprises an integrated circuit chip with a limited number of interface pins associated therewith for input/output functions.

5 5.(Currently Amended): The graphics processing engine of Claim 4, wherein said pins include an external memory access bus of a finite bit width for transferring data thereacross, and wherein said at least a portion of said plurality of memory blocks comprise embedded memory, and wherein said embedded memory is accessible with an effectively wider memory bus than said external memory bus to allow higher speed access thereto.

6.(Currently Amended): A graphics processing engine, comprising:  
a rendering engine processing core for receiving graphics primitives an incoming data stream and converting them to pixel information it to output information in a predetermined format for transfer to a display an output device, said rendering engine processing core operable to access memory locations with multiple memory access requests for a Read or a Write operation and operable in a first address space;

at least one memory, accessible by said rendering engine processing core and configured in a virtual address space different than said first address space;

10 a memory mapping device for mapping each of said memory requests to the virtual address space; and

a pipeline engine for pipelining said mapped memory access requests for both Read and Write operations in accordance with a predetermined pipelining scheme, said memory access requests received in parallel and processed asynchronously, such that said memory access requests can be delivered to said memory in an order different than said predetermined pipelining scheme.

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7.(Currently Amended): The graphics processing engine of Claim 6, wherein said rendering engine processing core, at least a portion of said memory, said memory mapping device and said pipeline engine are contained within a common bounded space with limited connectivity to external peripheral devices.

8.(Currently Amended): The graphics processing engine of Claim 6, wherein said memory includes at least one block of external memory external to said common bounded space.

9.(Currently Amended): The graphics processing engine of Claim 6, wherein said common bounded space comprises an integrated circuit chip with a limited number of interface pins associated therewith for input/output functions.

10.(Currently Amended): The graphics processing engine of Claim 9, wherein said pins include an external memory access bus of a finite bit width for transferring data thereacross, and wherein said at least a portion of said memory comprise embedded memory, and wherein said embedded memory is accessible with an effectively wider memory bus than said external memory bus to allow higher speed access thereto.

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